

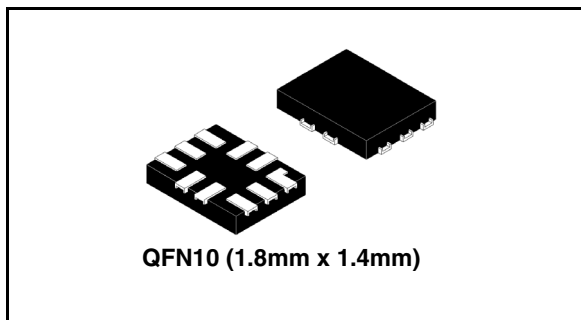


ST2G3236

2-bit dual supply bus transceiver level translator with a side series resistor

Features

- High speed:
 - $t_{PD} = 6.2\text{ns}$ (Max.) at $T_A = 85^\circ\text{C}$
 - $V_{CCB} = 1.8\text{V}$
 - $V_{CCA} = 3.3\text{V}$
- Low power dissipation:
 - $I_{CCA} = I_{CCB} = 5\mu\text{A}$ (Max.) at $T_A = 85^\circ\text{C}$
- Symmetrical output impedance:
 - $|I_{OHA}| = |I_{OLA}| = 7\text{mA}$ Min at $V_{CCA} = 2.75\text{V}$;
 $V_{CCB} = 1.65\text{V}$ or 2.3V
 - $|I_{OHB}| = |I_{OLB}| = 2\text{mA}$ Min at $V_{CCA} = 2.3\text{V}$
or 3.0V ; $V_{CCB} = 1.65\text{V}$
- Balanced propagation delays:
 - $T_{PLH} \approx T_{PHL}$
- Power down protections on inputs and outputs
- 26Ω series resistor on A side
- Operating voltage range:
 - V_{CCA} (OPR) = 1.4V to 3.6V
 - V_{CCB} (OPR) = 1.4V to 3.6V
- Max data rates:
 - 380Mbps (1.8V to 3.3V translation)
 - 260Mbps ($<1.8\text{V}$ to 3.3V translation)
 - 260Mbps (Translate to 2.5V)
 - 210Mbps (Translate to 1.5V)
- Latch-up performance exceeds 500mA (JESD17)
- ESD performance:
 - $\text{HBM} > 2\text{kV}$ (MIL STD 883 method 3015);
 - $\text{MM} > 200\text{V}$



Description

The ST2G3236 is a dual supply low voltage CMOS 2-bit Bus Transceiver fabricated with sub-micron silicon gate and five-layer metal wiring C2MOS technology. Designed for use as an interface between a 3.3V bus and a 2.5V or 1.8V bus in a mixed $3.3\text{V}/1.8\text{V}$, $3.3\text{V}/2.5\text{V}$ and $2.5\text{V}/1.8\text{V}$ supply systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This IC is intended for two-way asynchronous communication between data buses and the direction of data transmission is determined by DIR inputs. The A-port interfaces with the 3V bus, the B-port with the 2.5V and 1.8V bus.

All inputs are equipped with protection circuits against static discharge, giving them 2kV ESD immunity and transient excess voltage.

Order codes

Part number	Package	Packaging
ST2G3236	QFN10 (1.8mm x 1.4mm)	Tape and Reel

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1 Logic diagram and I/O equivalent circuit

Figure 1. Logic diagram

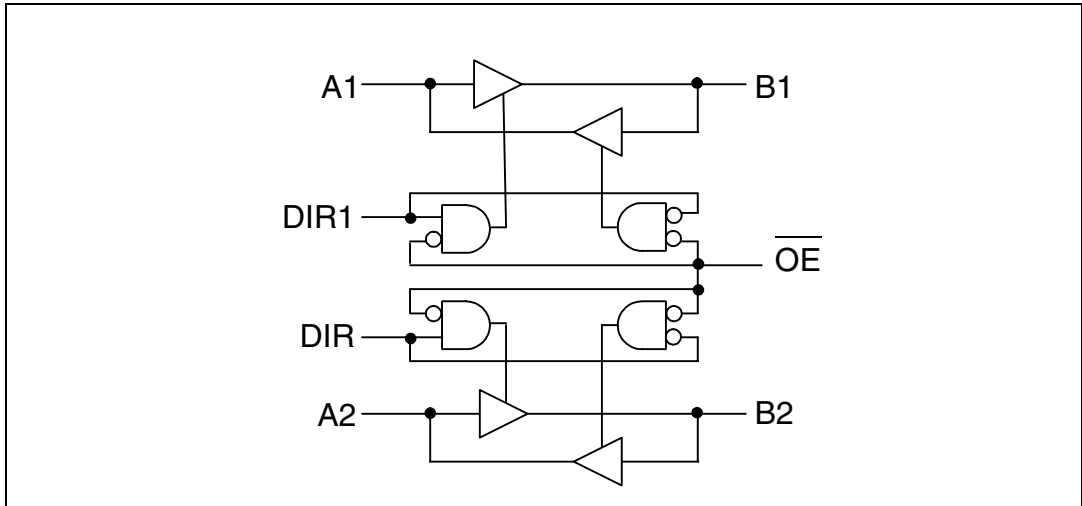
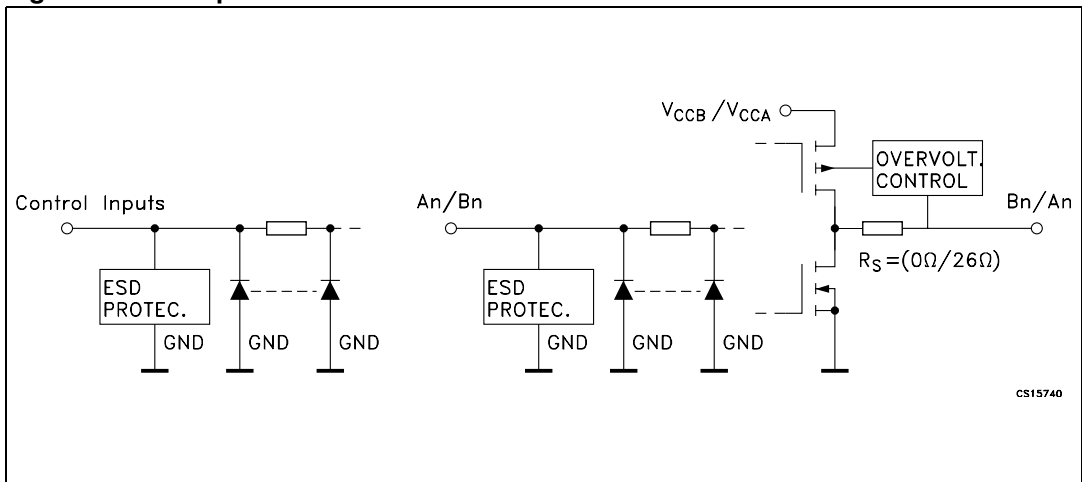


Figure 2. I/O equivalent circuit



1.1 Truth table

Table 1. Truth table

Inputs		Function		Output
\overline{OE}	DIRn	A BUS	B BUS	
L	L	Output	Input	B => A
L	H	Input	Output	B <= A
H	X	High-Z	High-Z	HIGH-Z

1.2 Recommended power-up sequence is as follows:

1. Apply power to either V_{CC}
2. Apply power to the \overline{OE} input and to the respective data inputs. This may occur at the same time as Step 1.
3. Apply power to other V_{CC}
4. Drive the \overline{OE} input LOW to enable the device.

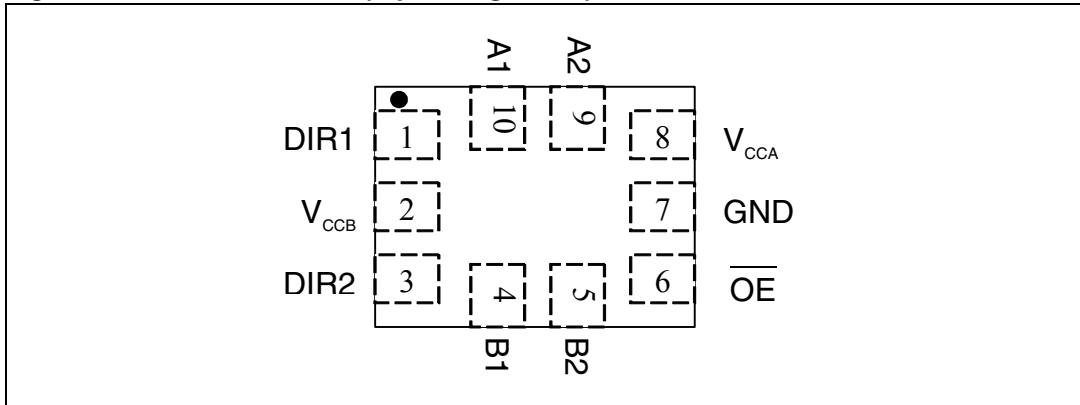
1.3 The recommended power-down sequence is as follows:

1. Drive \overline{OE} input HIGH to disable the device
2. Remove power from either V_{CC}
3. Remove power from other V_{CC}

2 Pin settings

2.1 Pin connections

Figure 3. Pin connections (top through view)



2.2 Pin descriptions

Table 2. Pin descriptions

Pin N°	Symbol	Name and function
1, 3	DIR1, DIR2	Directional controls
10	A1	Data inputs/outputs
4	B1	Data outputs/inputs
9	A2	Data inputs/outputs
5	B2	Data outputs/inputs
7	GND	Ground (0V)
8	V _{CCA}	Positive supply voltage
2	V _{CCB}	Positive supply voltage
6	$\overline{\text{OE}}$	Output enable (active low)

3 Electrical ratings

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltage	-0.5 to 4.6	V
V_{CCB}	Supply voltage	-0.5 to 4.6	V
V_I	DC input voltage	-0.5 to 4.6	V
$V_{I/OA}$	DC I/O voltage (output disabled)	-0.5 to 4.6	V
$V_{I/OB}$	DC I/O voltage (output disabled)	-0.5 to 4.6	V
$V_{I/OA}$	DC output voltage	-0.5 to $V_{CCA} + 0.5$	V
$V_{I/OB}$	DC output voltage	-0.5 to $V_{CCB} + 0.5$	V
I_{IK}	DC input diode current	-20	mA
I_{OK}	DC output diode current	-50	mA
I_{OA}	DC output current	± 50	mA
I_{OB}	DC output current	± 50	mA
I_{CCA}	DC V_{CC} or ground current	± 100	mA
I_{CCB}	DC V_{CC} or ground current	± 100	mA
P_D	Power dissipation	200	mW
T_{stg}	Storage temperature	-65 to +150	$^{\circ}\text{C}$
T_L	Lead temperature (10 sec)	260	$^{\circ}\text{C}$

Table 4. Recommended operating conditions

Symbol	Parameter	Value	Unit	
V_{CCA}	Supply voltage	1.4 to 3.6	V	
V_{CCB}	Supply voltage	1.4 to 3.6	V	
V_I	Input voltage (DIRn, \overline{OE})	0 to V_{CCA}	V	
$V_{I/OA}$	I/O voltage	0 to V_{CCA}	V	
$V_{I/OB}$	I/O voltage	0 to V_{CCB}	V	
T_{op}	Operating temperature	-40 to +85	$^{\circ}\text{C}$	
dt/dv	Input rise and fall time ⁽¹⁾	$V_{CCB} = 3.0$ to 3.6V	0 to 10	ns/V
		$V_{CCB} = 2.3$ to 2.7V	0 to 20	ns/V
		$V_{CCB} = 1.4$ to 1.95V	0 to 100	ns/V

1. V_{IN} from 0.8V to 2.0V at $V_{CC} = 3.0\text{V}$

4 Electrical characteristics

4.1 DC electrical characteristics for V_{CCA}

Table 5. DC specification for V_{CCA}

Symbol	Parameter	Test conditions			Value				Unit
		$V_{CCB}^{(1)}$ (V)	$V_{CCA}^{(1)}$ (V)		$T_A = 25^\circ\text{C}$		-40 to 85°C		
					Min	Max	Min	Max	
V_{IHA}	High level input voltage (An)	1.4 to 3.3V	1.4		$0.65V_{CCA}$		$0.65V_{CCA}$		V
			1.8		$0.65V_{CCA}$		$0.65V_{CCA}$		
			2.5		1.6		1.6		
			3.3		2.0		2.0		
V_{ILA}	Low level input voltage (An)	1.4 to 3.3V	1.4			$0.35V_{CCA}$		$0.35V_{CCA}$	V
			1.8			$0.35V_{CCA}$		$0.35V_{CCA}$	
			2.5			0.7		0.7	
			3.3			0.8		0.8	
V_{OHA}	High level output voltage	1.4 to 3.3V	1.4	$I_O = -100\mu\text{A}$	1.2		1.2		V
			2.75	$I_O = -0.4\text{mA}$	2.5		2.5		
			2.75	$I_O = -7\text{mA}$	2.2		2.2		
			2.3	$I_O = -5\text{mA}$	1.8		1.8		
			1.65	$I_O = -2\text{mA}$	1.4		1.4		
			1.4	$I_O = -1\text{mA}$	1.1		1.1		
V_{OLA}	Low level output voltage	1.4 to 3.3V	1.4	$I_O = 100\mu\text{A}$		0.20		0.20	V
			2.75	$I_O = 1\text{mA}$		0.40		0.40	
			2.75	$I_O = 7\text{mA}$		0.55		0.55	
			2.3	$I_O = 5\text{mA}$		0.40		0.40	
			1.65	$I_O = 2\text{mA}$		0.25		0.25	
			1.4	$I_O = 1\text{mA}$		0.20		0.20	
I_{IA}	Input leakage current	2.7	3.3	$V_I = V_{CC}$ or GND		± 0.5		± 5	μA
		1.4	2.7	$V_I = 3.6\text{V}$ or GND		± 0.5		± 5	
I_{OZA}	High impedance output leakage current	2.7	3.3	$V_{IA} = \text{GND}$ or 3.6V $V_{IB} = V_{IHB}$ or V_{ILB} $\overline{\text{OE}} = V_{CCB}$		± 1.0		± 10	μA

Table 5. DC specification for V_{CCA}

Symbol	Parameter	Test conditions			Value				Unit
		V _{CCB} ⁽¹⁾ (V)	V _{CCA} ⁽¹⁾ (V)		T _A = 25°C		-40 to 85°C		
					Min	Max	Min	Max	
I _{OFF}	Power OFF leakage current	0	0	V _{IA} =GND to 3.6V V _{IB} =GND to 3.6V \overline{OE} , DIR=GND to 3.6V		±1.0		±10	μA
I _{CCtA}	Quiescent supply current	1.95	2.7	V _{IA} =V _{CCA} or GND V _{IB} =V _{CCB} or GND		0.5		5	μA
		1.95	3.3						
		2.7	3.3						
ΔI _{CCtA}	Maximum quiescent supply current / input (An)	1.95	2.7	V _{IA} =V _{CCA} -0.6V V _{IB} =V _{CCB} or GND				0.75	mA
		1.95	3.3						
		2.7	3.3						

1. V_{CC} range = 3.3 ± 0.3; 2.5 ± 0.2V; 1.8 ± 0.15V

4.2 DC electrical characteristics for V_{CCB}

Table 6. DC specification for V_{CCB}

Symbol	Parameter	Test conditions			Value				Unit
		V _{CCB} ⁽¹⁾ (V)	V _{CCA} ⁽¹⁾ (V)		T _A = 25°C		-40 to 85°C		
					Min	Max	Min	Max	
V _{IHB}	High level input voltage (Bn, DIRn, \overline{OE})	1.4	1.4 to 3.3V		0.65V _{CCB}		0.65V _{CCB}		V
		1.8		0.65V _{CCB}		0.65V _{CCB}			
		2.5		1.6		1.6			
		3.3		2.0		2.0			
V _{ILB}	Low level input voltage (Bn, DIRn, \overline{OE})	1.4	1.4 to 3.3V		0.35V _{CCB}		0.35V _{CCB}		V
		1.8		0.35V _{CCB}		0.35V _{CCB}			
		2.5		0.7		0.7			
		3.3		0.8		0.8			

Table 6. DC specification for V_{CCB}

Symbol	Parameter	Test conditions			Value				Unit
		$V_{CCB}^{(1)}$ (V)	$V_{CCA}^{(1)}$ (V)		$T_A = 25^\circ\text{C}$		-40 to 85°C		
					Min	Max	Min	Max	
V_{OHB}	High level output voltage	1.4	1.4 to 3.3V	$I_O = -100\mu\text{A}$	1.3		1.3		V
		1.8		$I_O = -100\mu\text{A}$	1.6		1.6		
		2.75		$I_O = -20\text{mA}$	2.2		2.2		
		2.75		$I_O = -15\text{mA}$	1.7		1.7		
		2.3		$I_O = -4\text{mA}$	1.44		1.44		
		1.65		$I_O = -2\text{mA}$	1.5		1.5		
		1.4		$I_O = -2\text{mA}$	1.25		1.25		
V_{OLB}	Low level output voltage	1.4	1.4 to 3.3V	$I_O = 100\mu\text{A}$		0.1		0.1	V
		1.8		$I_O = 100\mu\text{A}$		0.2		0.2	
		2.75		$I_O = 20\text{mA}$		0.55		0.55	
		2.75		$I_O = 15\text{mA}$		0.35		0.35	
		2.3		$I_O = 4\text{mA}$		0.39		0.39	
		1.65		$I_O = 2\text{mA}$		0.20		0.20	
		1.4		$I_O = 2\text{mA}$		0.15		0.15	
I_{IB}	Input leakage current	2.7	3.3	$V_I = V_{CC}$ or GND		± 0.5		± 5	μA
		1.4	2.7	$V_I = 3.6\text{V}$ or GND		± 0.5		± 5	
I_{OZB}	High impedance output leakage current	2.7	3.3	$V_{IA} = V_{IHA}$ or V_{ILA} $V_{IB} = \text{GND}$ or 3.6V $\overline{OE} = V_{CCB}$		± 1.0		± 10	μA
I_{CCIB}	Quiescent supply current	1.95	2.7	$V_{IA} = V_{CCA}$ or GND $V_{IB} = V_{CCB}$ or GND		0.5		5	μA
		1.95	3.3						
		2.7	3.3						
ΔI_{CCIB}	Maximum quiescent supply current / input (B_n , DIR_n , \overline{OE})	1.95	2.7	$V_{IB} = V_{CCB} - 0.6\text{V}$ $V_{IA} = V_{CCA}$ or GND				0.75	mA
		1.95	3.3						
		2.7	3.3						

1. V_{CC} range = 3.3 ± 0.3 ; $2.5 \pm 0.2\text{V}$; $1.8 \pm 0.15\text{V}$

4.3 AC electrical characteristics

Table 7. AC electrical characteristics

Symbol	Parameter	Test condition			Value		Unit
		V _{CCB} (V)	V _{CCA} (V)		-40 to 85 °C		
					Min	Max	
t _{PLH} t _{PHL}	Propagation delay time An to Bn	1.8 ± 0.15	2.5 ± 0.2	C _L = 30pF R _L = 500Ω	1.0	5.8	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	6.2	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.4	
t _{PLH} t _{PHL}	Propagation delay time Bn to An	1.8 ± 0.15	2.5 ± 0.2	C _L = 30pF R _L = 500Ω	1.0	5.5	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	5.1	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.0	
t _{PZL} t _{PZH}	Output enable time \overline{OE} to An	1.8 ± 0.15	2.5 ± 0.2	C _L = 30pF R _L = 500Ω	1.0	5.4	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	5.1	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.0	
t _{PZL} t _{PZH}	Output enable time \overline{OE} to Bn	1.8 ± 0.15	2.5 ± 0.2	C _L = 30pF R _L = 500Ω	1.0	5.3	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	5.2	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.6	
t _{PLZ} t _{PHZ}	Output disable time \overline{OE} to An	1.8 ± 0.15	2.5 ± 0.2	C _L = 30pF R _L = 500Ω	1.0	5.2	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	5.6	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.8	
t _{PLZ} t _{PHZ}	Output disable time \overline{OE} to Bn	1.8 ± 0.15	2.5 ± 0.2	C _L = 30pF R _L = 500Ω	1.0	4.6	ns
		1.8 ± 0.15	3.3 ± 0.3		1.0	4.5	
		2.5 ± 0.2	3.3 ± 0.3		1.0	4.4	
t _{OSLH} t _{OSHL}	Output to output skew time ⁽¹⁾ ⁽²⁾	1.8 ± 0.15	2.5 ± 0.2	C _L = 30pF R _L = 500Ω		0.5	ns
		1.8 ± 0.15	3.3 ± 0.3			0.5	
		2.5 ± 0.2	3.3 ± 0.3			0.75	

1. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (T_{osH} = |t_{PLHm} - t_{PLHn}|, t_{osL} = |t_{PHLm} - t_{PHLn}|)
2. Parameter guaranteed by design

4.4 Capacitance characteristics

Table 8. Capacitance characteristics

Symbol	Parameter	Test Condition			Value					Unit
		V _{CCB} (V)	V _{CCA} (V)		T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
C _{INB}	Input capacitance	Open	Open			5				pF
C _{I/O}	Input/output capacitance	2.5	3.3			6				pF
C _{PD} (1)	Power dissipation capacitance	2.5	3.3	f=10MHz		29				pF
		1.8	3.3			29				

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average current can be obtained by the following equation. $I_{CC(opr)} - C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$ (per circuit)

5 Test circuit

Figure 4. Test circuit

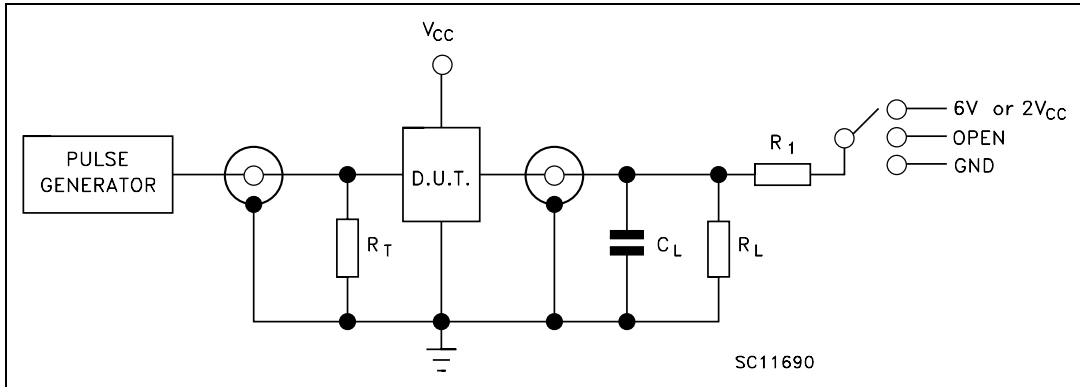


Table 9. Test values

Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ} ($V_{CC} = 3.0$ to $3.6V$)	6V
t_{PZL} , t_{PLZ} ($V_{CC} = 2.3$ to $2.7V$ or $V_{CC} = 1.6$ to $1.95V$)	$2V_{CC}$
t_{PZH} , t_{PHZ}	GND

6 Waveforms

Table 10. Waveform symbol value

Symbol	V _{CC}		
	3.0 to 3.6V	2.3 to 2.7V	1.65 to 1.95V
V _{IH}	V _{CC}	V _{CC}	V _{CC}
V _M	1.5V	V _{CC} /2	V _{CC} /2
V _X	V _{OL} + 0.3V	V _{OL} + 0.15V	V _{OL} + 0.15V
V _Y	V _{OL} - 0.3V	V _{OL} - 0.15V	V _{OL} - 0.15V

- C_L = 30pF or equivalent (includes jig and probe capacitance)
- R_L = R₁ = 500Ω or equivalent
- R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 5. Waveform - propagation delay (f = 1MHz, 50% duty cycle)

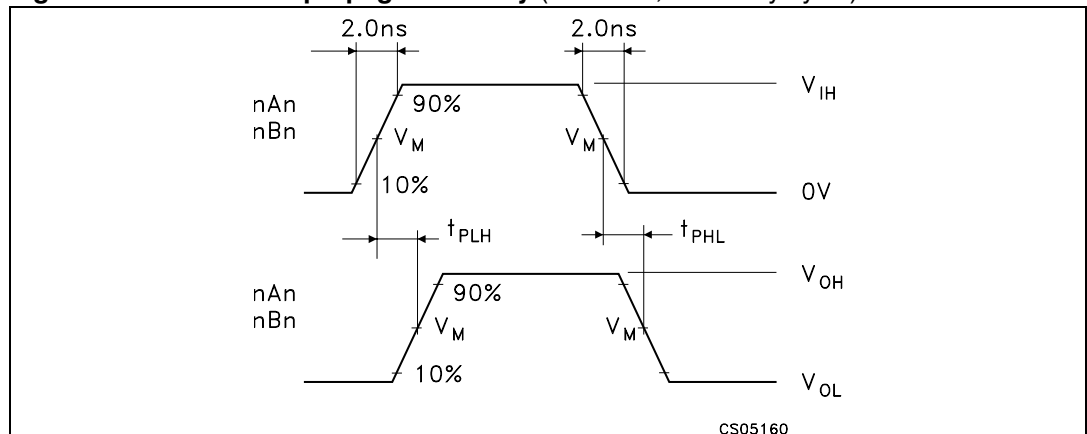
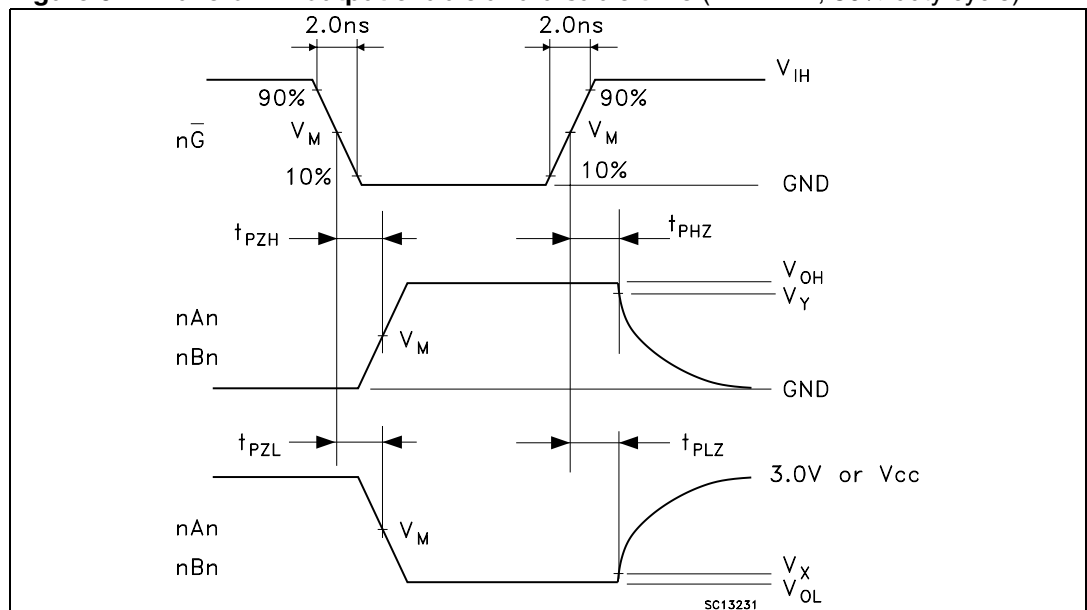


Figure 6. Waveform - output enable and disable time (f = 1MHz, 50% duty cycle)



7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 1. QFN10L(1.8x1.4) Mechical data

ref.	mm			inch		
	Nom	Min	Max	Nom	Min	Max
A	0.50	0.45	0.55	0.020	0.017	0.021
A1	0.02	0	0.05	0.001	0	0.002
A3	0.127			0.005	0	0
b	0.20	0.15	0.25	0.007	0.006	0.010
D	1.80	1.70	1.90	0.070	0.066	0.074
E	1.40	1.30	1.50	0.055	0.051	0.059
e	0.40			0.015		
L	0.40	0.30	0.50	0.015	0.011	0.020

Figure 7. Package dimension

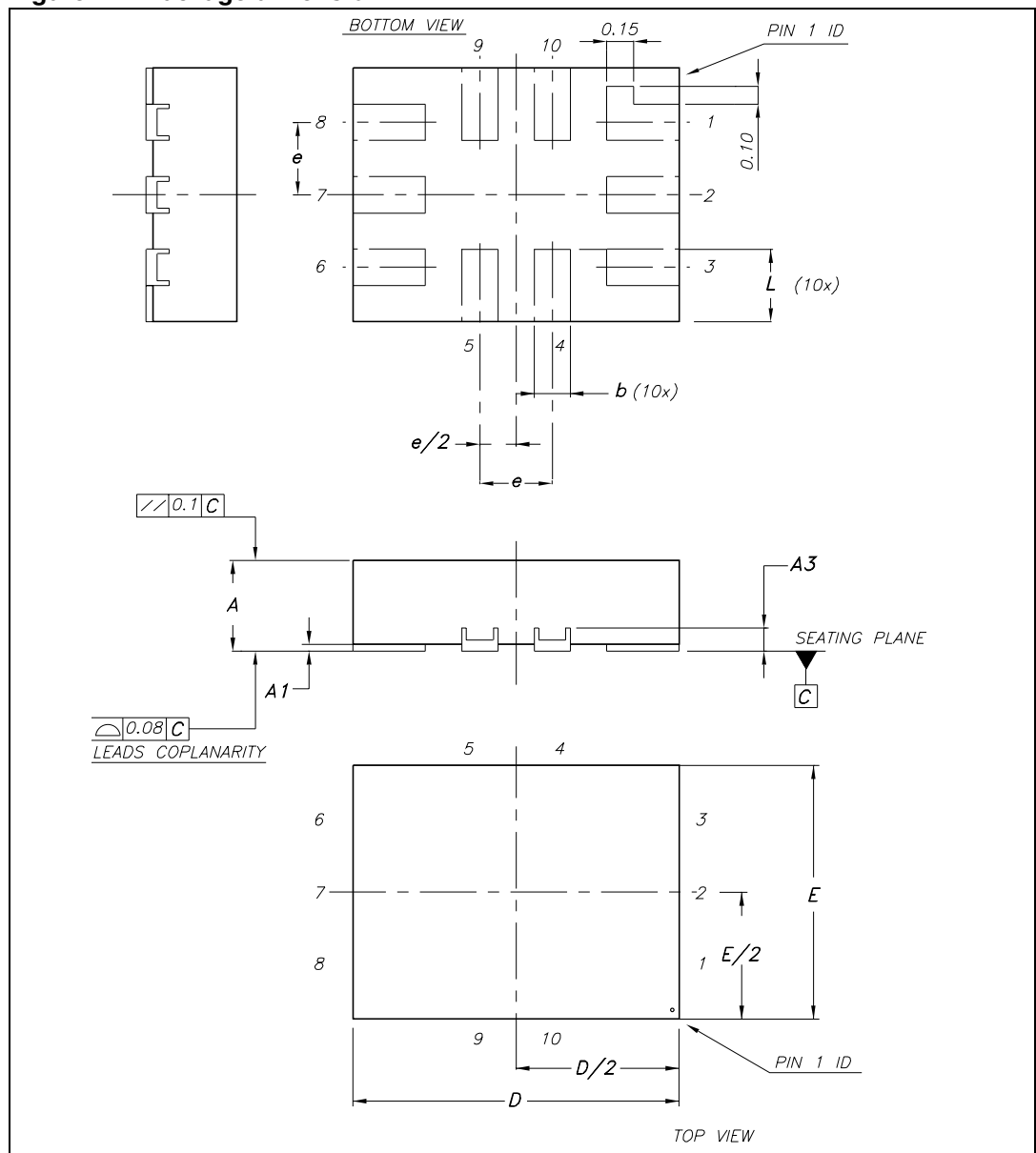


Figure 8. QFN10L(1.8x1.4) Foot print recommendation

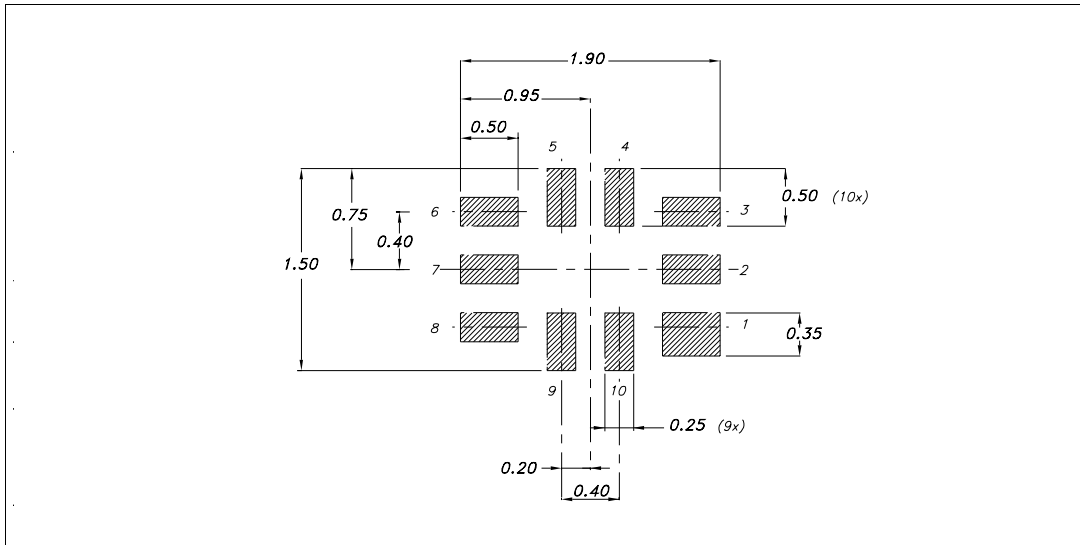


Figure 9. QFN10L(1.8x1.4) carrier type

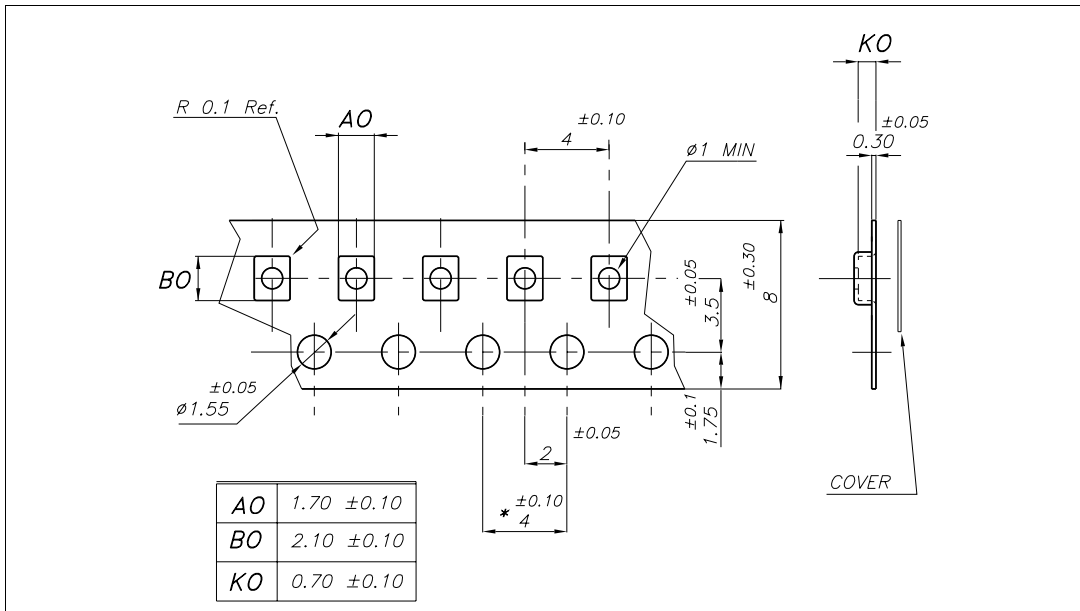


Figure 10. QFN10L(1.8x1.4) Reel information

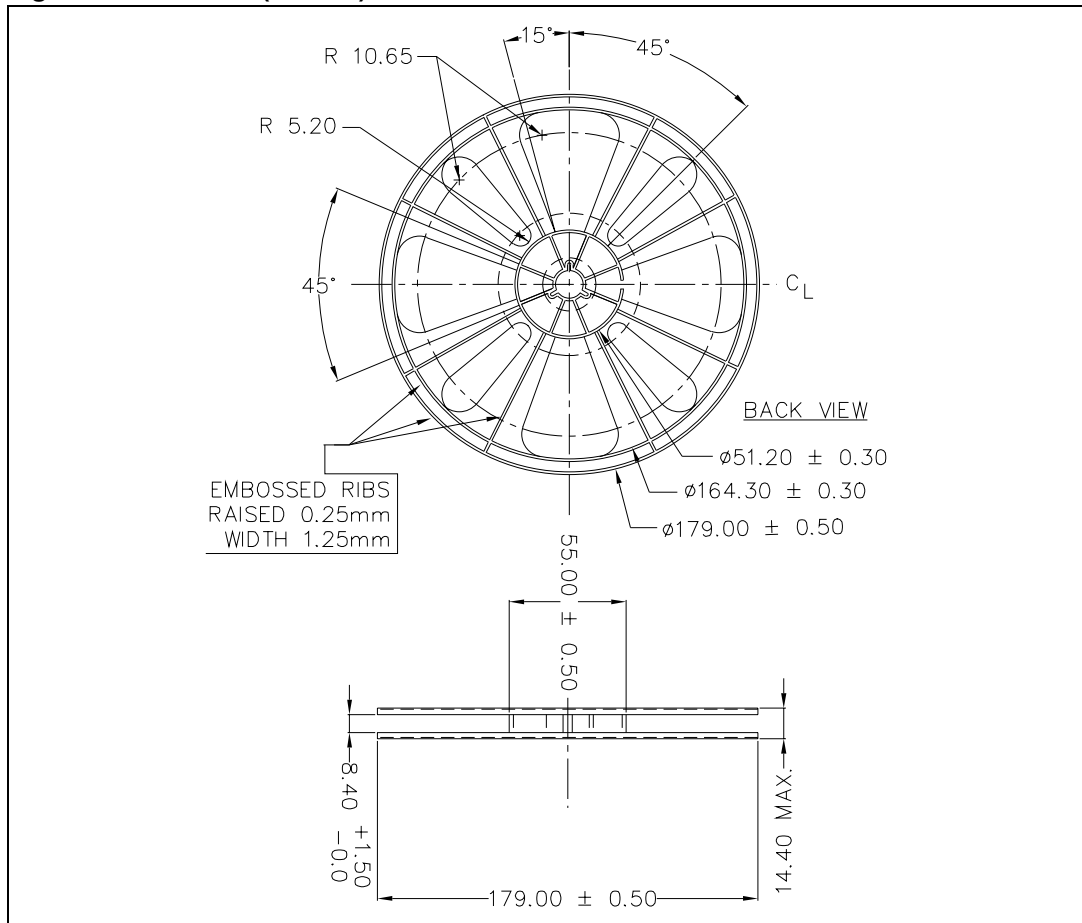
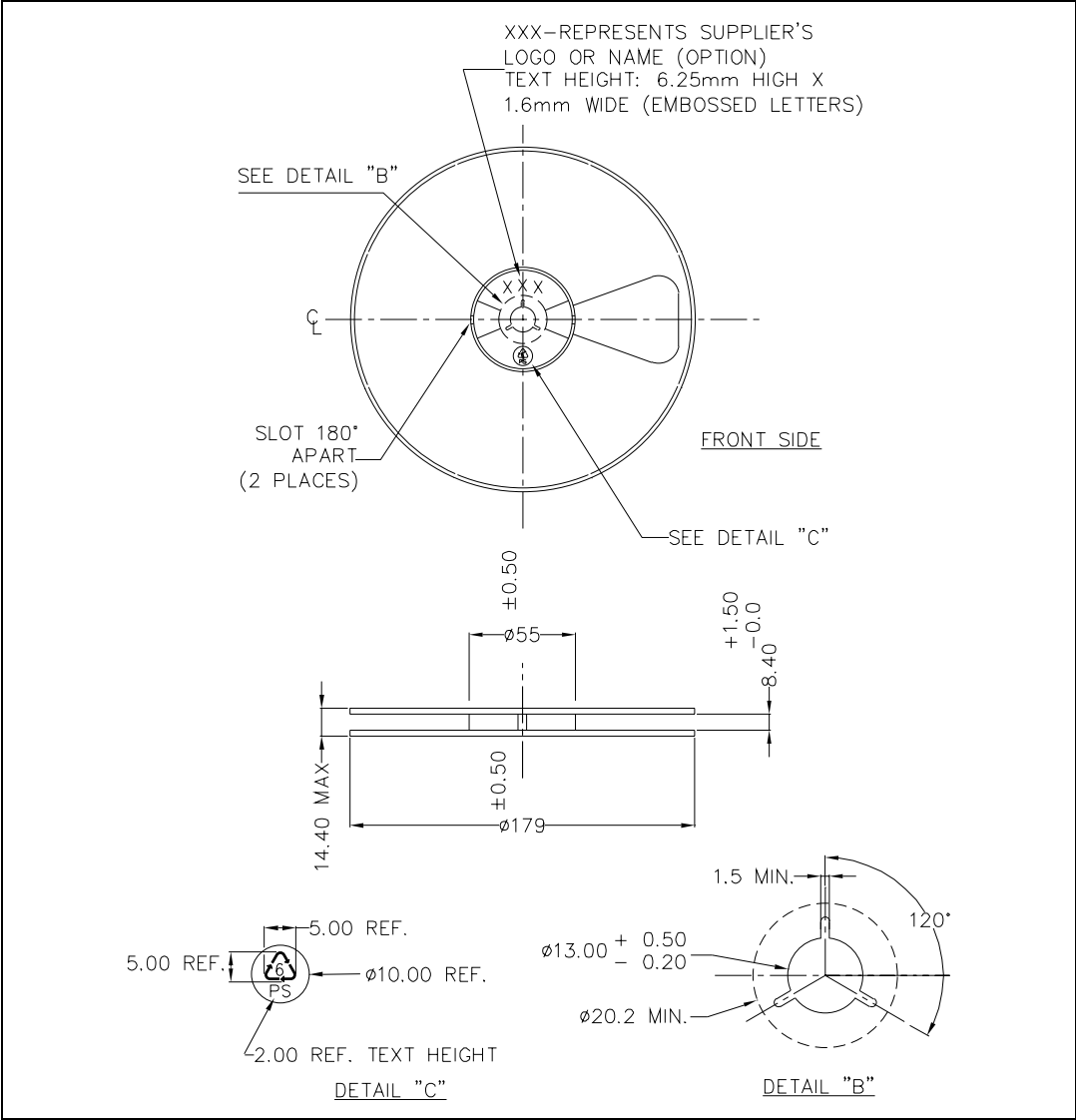


Figure 11. QFN10L(1.8x1.4) Reel information



8 Revision history

Table 11. Revision history

Date	Revision	Changes
06-Dec-2006	1	First release

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